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Brenda O. Holmes

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Comments

In re Application of: Makoto Yamamoto

Serial No.: 10/014,949

Art Unit: 2814

For: Lateral Transistor Having Graded Base Region,
Semiconductor Integrated Circuit And
Fabrication Method Thereof

*copy of
Amendment
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PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
Makoto Yamamoto)
Serial No. 10/014,949) Art Unit: 2814
Filed: October 26, 2001) Examiner: Shrinivas H. Rao
For: Lateral Transistor Having Graded Base Region,) FAX RECEIVED
Semiconductor Integrated Circuit And)
Fabrication Method Thereof) DEC 10 2003

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SUPPLEMENTAL AMENDMENT AND INTERVIEW SUMMARY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

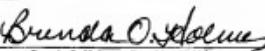
Sir:

Please reconsider the application in light of the following amendment.

AMENDMENT

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

I hereby certify that this correspondence is being transmitted to United States Patent and Trademark Office via facsimile no. 703.746.3926 on December 10, 2003.


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